IRRIGATION SYSTEM FOR AGRICULTURE

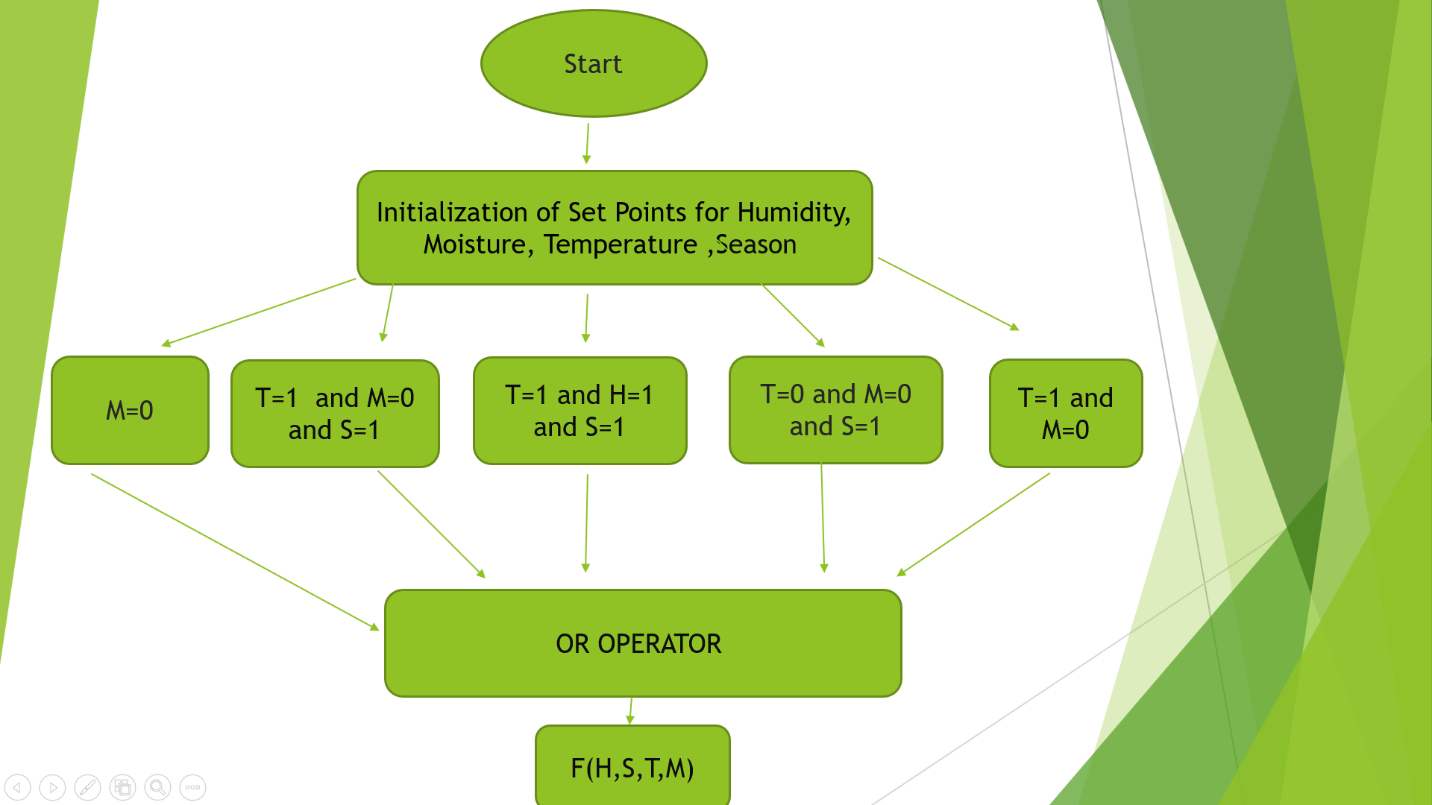
AIM :-

To design and implement circuit for Irrigation System for Agriculture using Verilog HDL.

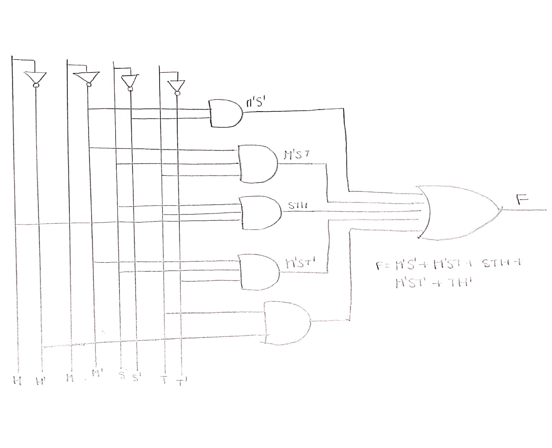
TOOL :-

Xilinx ISE 9.2i Version

|  |  |
| --- | --- |
| FAMILY | SPARTAN 3 |
| Device | XC3S400 |
| Package | PQ208 |
| Speed | -4/-5 |
| Synthesis | XST(VERILOG/VHDL) |
| Simulator | ISE Simulator |

ALGORITHM :- 

BLOCK DIAGRAM :-



LOGIC :-

* According to the algorithm we can generate the logic to implement the circuit. The functional logic to implement would be:

Output (F) =F(H,S,T,M)=M'S' + M'ST + STH + M'ST' + TH'

SOURCE CODE :-

module IrrigationSystemforAgriculture(T,S,H,M,F);

input T,S,M,H;

output F;

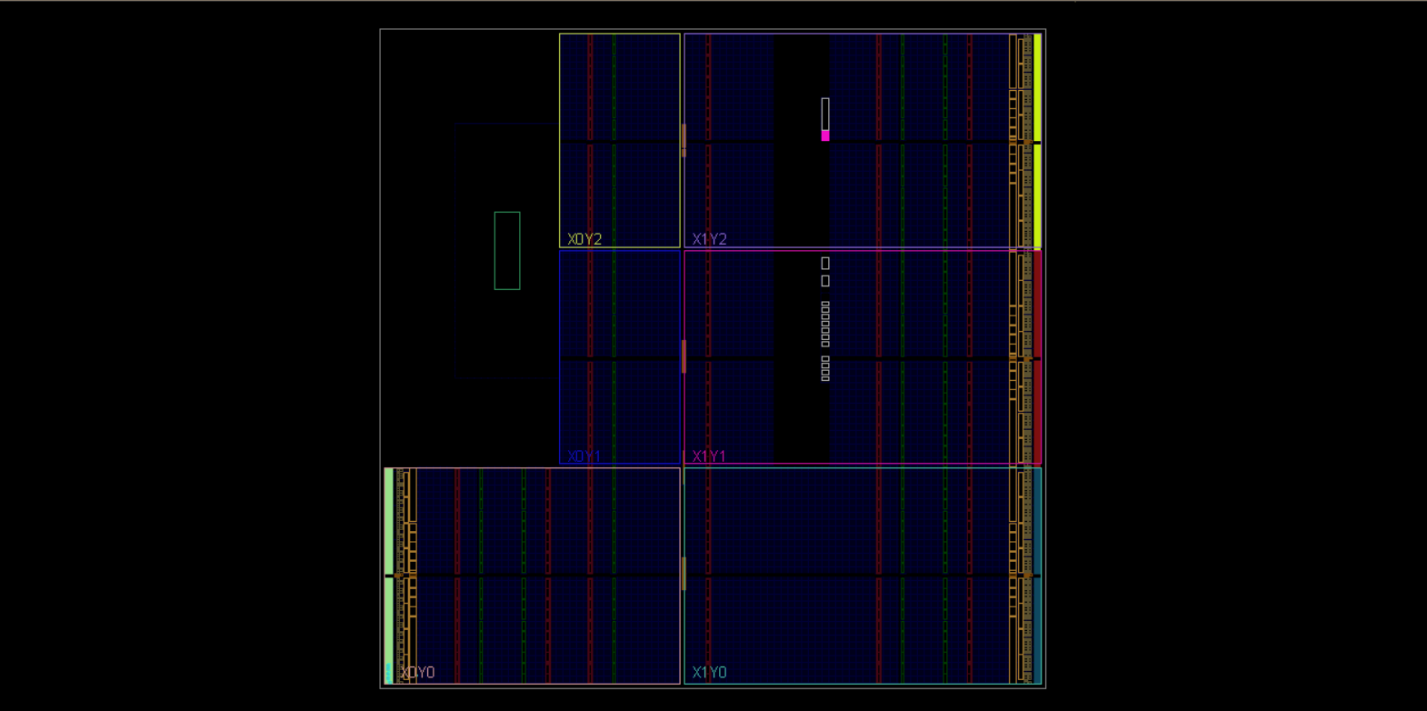
assign F = ~M & ~S | ~M & S & T | S& T & H| ~M & S & ~T| T & ~H ;

endmodule

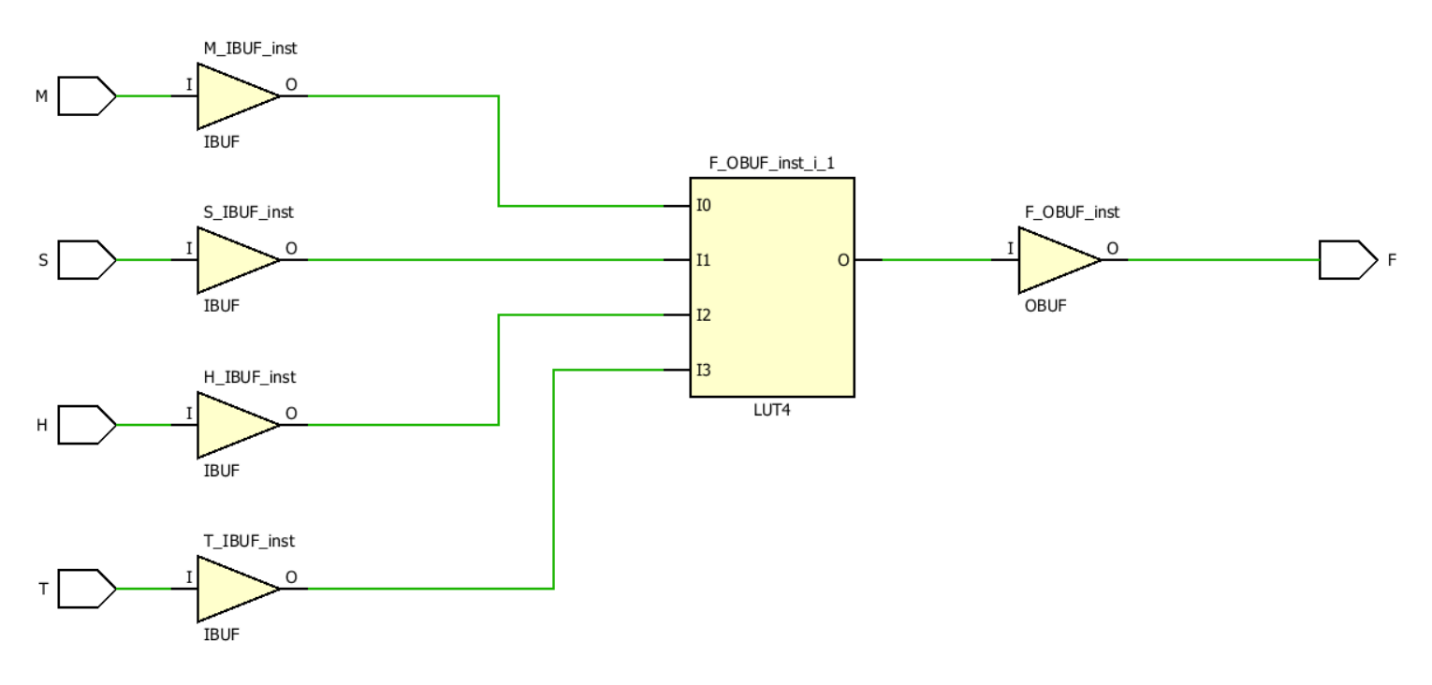
CIRCUIT :-

We use ZED Board as the base board to etch the circuit.

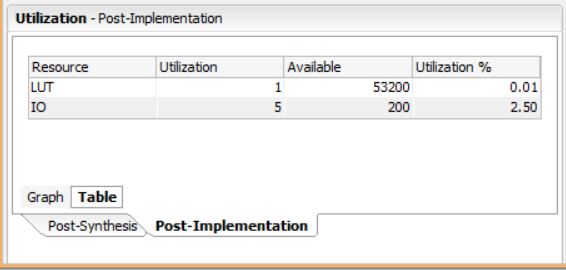
ZED BOARD CIRCUIT DESIGN :-



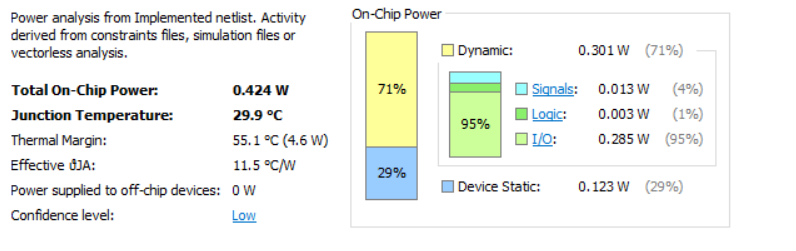
IMPLEMENTED RTL SCHEMATIC DESIGN :-



DEVICE UTILISATION :-



DEVICE POWER UTILISATION :-



CONCLUSION :-

The Irrigation System for Agriculture is designed and implemented using Verilog HDL.